

System On Chip: Taking the “Hard” out of Hardware

By John S. Rinaldi

Only a short time ago building a completely customized single-chip solution for an embedded application was a risky and expensive process. A missed feature or a misread of the market requirements was more than just a headache. More than likely the product development team would be working on new resumes as their next project. The process of designing ASICs (Application Specific Integrated Circuits) required an incredible amount of foresight into the customer requirements and target market. Respinning silicon after rollout meant disaster, lost market share and a financial doomsday. And the process has not improved. As chip densities have soared, ASIC development is now even more cumbersome, risky and pricey. Only the largest companies can afford the time, development costs and risk for anything but the largest volume applications.

Lucky for us product developers, an entire market of configurable processor architectures has arrived to meet the need of embedded solutions: flexibility, performance, low cost, fast time to market and product differentiation. Several types of these solutions are available including Soft Instruction processors, Configurable Processors and combo processors implementing aspects of both Soft Instruction processors and Configurable Processors.

Soft Instruction processor architectures allow a designer to customize the CPU architecture. The specific instructions supported, the peripherals available to it and the number of registers are just some ways these devices can be tailored for your application. Some vendors provide mechanisms to add, delete and create highly tailored instructions. Design packages for these architectures sometimes include performance tools with instant feedback on the performance, die size and power requirements of a particular design. With the final architecture residing in silicon, these types of architectures are well suited for high volume, low cost applications which formerly would have used ASICs.

Configurable processors, also known as System on Chip processor architectures, are FPGA based. In these architectures, standard and customer-derived logic engines can be easily added, modified and extended as needed. By moving discrete logic functionality to internal FPGA the designer gets a highly flexible logic solver, based around a standard processor core. With FPGA logic instead of foundry logic, the logic can be easily revised at any point in the design cycle. “Specials” or custom logic configurations can be quickly created for potential new customers driving down the batch size to single unit quantities.

Selecting an architecture, tool set and methodology from the wide range of configurable processor solutions is both a huge technical and product challenge. Let’s look at some of the more important questions that the product design team should ask:

Where are we on the volume/flexibility curve?

A very high volume application usually requires specific performance and cost targets. Flexibility is a minor consideration if it is considered at all. These types of applications will most likely be most effectively deployed using ASIC technology generated from the analysis and development tools offered by the Soft Instruction processor vendors. These tools generate highly tailored, highly specialized, mass producible dies using the set of instructions and components selected by the designer.

Lower volume applications usually require much greater flexibility, are less cost sensitive and can tolerate a wider performance window. These types of applications are much more appropriate for the configurable processor architectures. With the ability to quickly and easily modify hardware logic right up until production, these designs are more flexible to quickly meet the changing needs of highly fluid target markets.

How critical is performance and what kind of performance is important?

There is a great difference in the performance attained by processor algorithms, FPGA logic engines and discrete logic. If you have critical custom algorithms they will run more slowly as software algorithms than as a long FPGA logic pipeline in a configurable processor. If discrete logic resolution is an issue, discrete logic can be resolved much faster than FPGA. In some cases, the customizable instruction set of a Soft Instruction processor can yield a magnitude increase in performance over other implementations. Understanding and benchmarking the performance requirements of your application is required before selecting a SoC solution with the proper performance.

Is DSP a requirement?

Many more applications now require the integration of DSP technology with standard processor functions. If this is required by your application, the Soft Instruction processor architectures typically have DSP functions which can be optionally integrated into the processor core.

Does your design require readily available standard components?

If your application uses a number of common peripherals (UARTs, Timers, interrupt logic) or specialized components (such as an LCD Display interfaces) a configurable processor can not only accelerate your product development but reduce your PCB real estate, component count and one-time NRE costs.

How important and sophisticated are the vendors troubleshooting capabilities?

If you are designing a highly reusable product, the debug capabilities offered become extremely important. How easily can you connect to the system? What kinds of specialized software are required? Since you won't be using it on an everyday basis, can a novice get up to speed quickly and troubleshoot the design without extensive training? If your product is on the high volume/low flexibility curve, the vendors troubleshooting capabilities are much less important.

Future articles in this series will focus on using SoC architectures in PC/104 designs and reviews of the various vendors offering solutions to developers in this growing market.

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